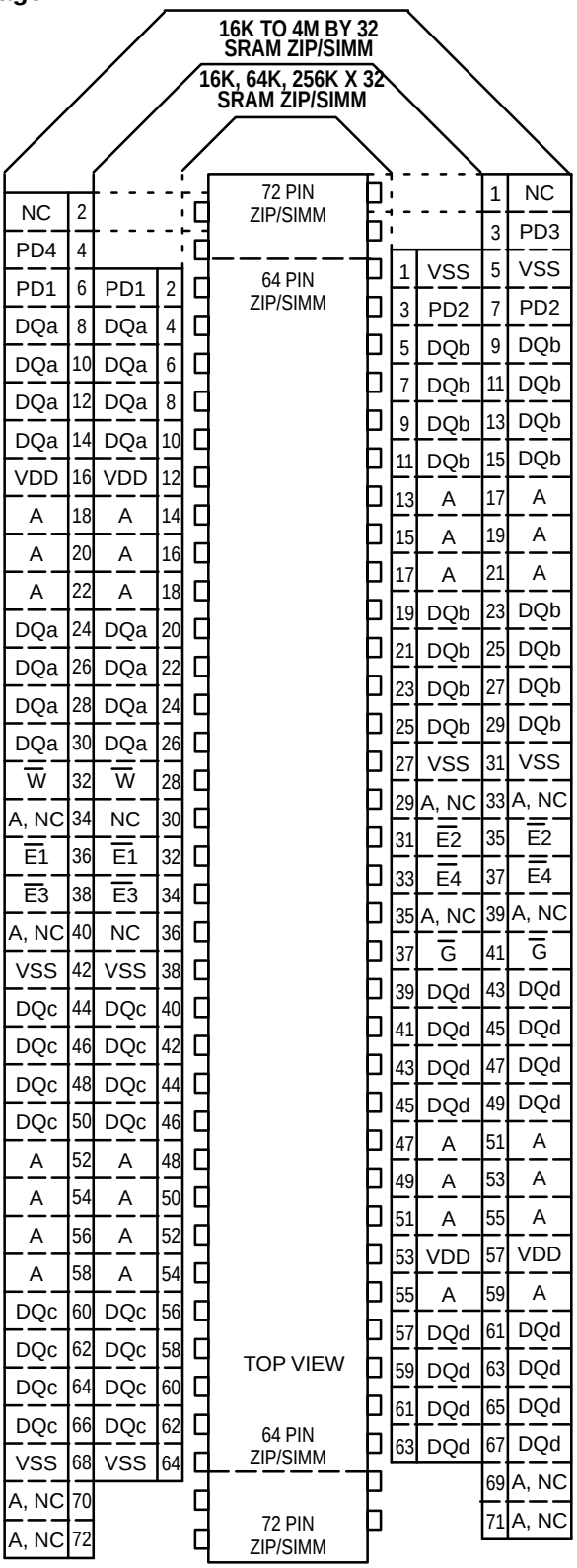
## 4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

CAPACITY—16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, or 4M WORDS OF 32 BITS
CONFIGURATION—FOUR BANK MODULE
—SELECTABLE BY BYTE GROUPS
LOGIC FEATURE—The 72 pin modules are supersets of the 64 pin family with added capacity.
PACKAGE—64 and 72 PIN SIP MODULEWITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.4.1–1




NOTES for 72–pin ZIP/SIMM module pinout:
1. $\overline{E1}$ enables DQa pins 8, 10, 12, 14, and 24, 26, 28, 30; $\overline{E2}$ enables DQb pins 9, 11, 13, 15, and 23, 25, 27, 29; $\overline{E3}$ enables DQc pins 44, 46, 48, 50, and 60, 62, 64, 66; $\overline{E4}$ enables DQd pins 43, 45, 47, 49, and 61, 63, 65, 67.
2. $\overline{W}$ enables writing into all enabled devices.
3. $\overline{G}$ enables outputs from any and all enabled devices.
4. This footprint is a superset of the 64–pin JEDEC standard. Any 64 pin JEDEC standard module may be used in the 72–pin footprint. PD3 and PD4 become NC (OPEN) in this case.
5. Two pins (1 & 2) are available for future definition.

**PRESENCE DETECT TRUTH TABLE**

| MOD CONFIG | PD4 | PD3 | PD2 | PD1 |
|---|---|---|---|---|
| 72P MOD | PIN 68 | PIN 67 | PIN 66 | PIN 11 |
| # 16K X 32 | O | O | O | S |
| 32K X 32 | S | S | O | O |
| # 64K X 32 | O | O | S | O |
| 128K X 32 | S | O | O | O |
| # 256K X 32 | O | O | S | S |
| 512K X 32 | O | S | O | O |
| 1M X 32 | O | S | O | S |
| 2M X 32 | O | S | S | O |
| 4M X 32 | O | S | S | S |

O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS

# Indicates configurations duplicated in 64P package. Use PD1 & PD2 only.

PRESENCE DETECT NOTES
1. Compatibility has been maintained with existing 64–pin standard
2. PD signature has been added for 32K X 32 & 128K X 32 configurations that were not implemented in the 64–pin standard.
3. Six PD signatures are left undefined for future definition.

**ADDRESS PIN ASSIGNMENTS**

| CONFIGURATION | ADDRESS PIN NUMBER | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 72 P MODULES | 33 | 34 | 40 | 39 | 69 | 70 | 71 | 72 |
| 16K X 32 | NC | NC | NC | NC | NC | NC | NC | NC |
| 32K X 32 | A | NC | NC | NC | NC | NC | NC | NC |
| 64K X 32 | A | A | NC | NC | NC | NC | NC | NC |
| 128K X 32 | A | A | A | NC | NC | NC | NC | NC |
| 256K X 32 | A | A | A | A | NC | NC | NC | NC |
| 512K X 32 | A | A | A | A | A | NC | NC | NC |
| 1M X 32 | A | A | A | A | A | A | NC | NC |
| 2M X 32 | A | A | A | A | A | A | A | NC |
| 4M X 32 | A | A | A | A | A | A | A | A |
| 64 P MODULES | 29 | 30 | 35 | 36 | | | | |
| 16K X 32 | NC | NC | NC | NC | | | | |
| 64K X 32 | A | A | NC | NC | | | | |
| 256K X 32 | A | A | A | A | | | | |

## FIGURE 4.4.1–1
## 16K TO 4M BY 32 SRAM ZIP/SIMM MODULE